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Meeting #2

Considerations For Testing Enhanced Squitter Detection Techniques

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Summary

Appendix I discusses the following Enhanced Squitter Detection Techniques: Preamble Detection, Bit Value and Confidence Declaration, and Error Correction.

Each Category of enhancement should be tested independently. This is to ensure that each of the enhancements are correctly implemented. While each enhancement will provide improved reply reception in environments where interference is present, each enhancement is unique in what type of interference environment it is most effective in improving reply reception.

Considerations For Testing Enhanced Squitter Detection Techniques

Appendix I discusses the following Enhanced Squitter Detection Techniques.

Preamble Detection
Standard (four Pulse) Preamble Detection
Nine Pulse Preamble Detection
Dual Preamble Detector / Retriggerable Preamble Detector

Bit Value and Confidence Declaration
Center Sample Method
Center Amplitude Method
Multiple Sample Method

Error Correction
Conservative/Whole Reply Technique
Whole Reply Technique
Brute Force Technique

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Preamble Detection

Correct Preamble detection is necessary to start the Mode S reply processor when a reply is received. Three types of interference affect correct preamble detection.

1. Overlapping pulses that cause the preamble pulses to be elongated,
2. Overlapping ATCRBS replies that line up to look like a Mode S reply preamble and
3. Overlapping Mode S replies.

The first type of interference may cause a preamble to go undetected and result in a missed Mode S message. This type of interference is minimized by implementing the Standard Preamble Detection Method described in the DO185A MOPS.

The second and third types are minimized by the Nine Pulse Preamble Detection method and the Dual/Retriggerable Preamble Detector respectively.

The second type of interference can cause detection of a false preamble. This activates the Mode S reply processor which may then process garbage for 112 us and miss any real messages received during that time. This effect is minimized by the Nine Pulse Preamble Detection method.

The third type of interference (When Mode S replies overlap and the second reply is a higher power level than the first, the first message will likely be corrupted to the point that it cannot be decoded. if a real preamble is detected and reply processing activated and a second higher level Mode S reply message overlaps the first it will very likely corrupt the first message making it unrecognizable.

Preamble Detection Tests

Standard (four Pulse) Preamble Detection
Test as per DO-185A

Nine Pulse Preamble Detection
Verify that occurrence of power in either chip of first 5 data bits allows preamble detection.
Verify that absence of power in both chips of any one of the first 5 data bits inhibits preamble detection.

Dual Preamble Detector / Retriggerable Preamble Detector
Verify that a higher power overlapping squitter is detected.

Bit Value and Confidence Declaration

Interference pulses can cause the value of a specific bit or the confidence of that bit to be incorrectly determined. Overlapping ATCRBS replies are a common cause of interference and depending on the power of the interference relative to the Mode S message level will have a different effect on the bit value and confidence declaration. Interference with power lower than the message (<6 db) will have little or no effect. When using the center sample method, interference of higher power will cause incorrect declaration. When using the Center Amplitude of Mutiple Sample methods. interference that is very close in power to the reply message will have greater effect than interference that is greater than (>3 db) or less than (< 3db) the reply power level. The positioning of the interference also plays a role in determining whether or not the bit will be correctly decoded.

Bit Value and Confidence Declaration Tests

Testing should be performed to show that the designed implementation is functioning correctly. The capability to view bit values and confidence or to disable error correction is necessary to ensure that bits are being correctly declared and not subsequently corrected.

Center Sample Method

Insert an overlapping pulse and move it through the 1 us data bit. Verify that for each sample position the bit value and confidence are declared as follows:

Relative Position of Interference (microseconds)	Normal Bit Value	Interference Power	Bit Value	Confidence
0	1	+1	1	High
0.125	1	+1	1	High
0.250	1	+1	1	Low
0.375	1	+1	0	Low
0.500	1	+1	0	Low
0	1	-1	1	High
0.125	1	-1	1	High
0.250	1	-1	1	Low
0.375	1	-1	1	Low
0.500	1	-1	1	Low

Center Amplitude Method

Test with interfering pulses at higher and lower power such that the power level of the energy in the '1' and '0' chips is as per the following table. Verify correct bit value and confidence.

Power Relative to Preamble		Bit Value	Confidence
'1' Chip	'0' Chip		
0	+4	1	High
0	-4	1	High
-4	+4	0	Low
+1	-1	1	Low
+4	0	0	High
-4	0	0	High
+4	-4	1	Low
-1	+1	0	Low

Multiple Sample Method

Simulate interference within the 1 microsecond data bit and verify the bit value and confidence are declared correctly.

Interference Power Relative to Preamble	Data Pulse Power Relative to Preamble	Relative Position of Interference	Normal Bit Value	Declared Bit Value	Declared Confidence
+2	0	0.5	1	?	Low
+4	0	0.5	1	1	High
-4	0	0.5	1	1	High
-7	+4	0.5	1	1	High
-2	0	0.5	0	?	Low
+4	0	0.5	0	1	High
-4	0	0.5	0	1	High
-7	+4	0.5	0	1	High

Error Correction

Error Correction provides a method to determine if a bit in a Mode S message may be in error and then correct it if it is.

Error Correction Tests

In order to test error correction algorithms it is necessary to ensure that bit values and confidence levels are declared to require error correction to take place.

Conservative Technique
Test per DO185A

Whole Reply Technique
Verify that with five ATCRBS replies overlapping an Extended Squitter but not overlapping each other the message can be correctly decoded. The interfering replies should be varied in amplitude and position to determine the reply reception probability.

Brute Force Technique
Similar to the Whole Reply Technique.

Combination of Enhancement Methods

An overall test should be performed to characterize receiver performance in a high FRUIT environment. This could be done by simulating extended squitters overlapped by Random FRUIT or by overlapping the squitter with FRUIT messages that are slowly moved through the messages. The reply reception probability would be used to determine the overall effectiveness of the reply processsor. The percentages in the table below show the results of one such test performed at Lincoln Laboratories. Flight testing would also be a means of determining reply reception probabilities in High FRUIT environments.

	Error Correction Algorithm Employed			
Amplitude Information	None	Conservative	Whole Reply	Brute Force @5
None	**3**	**8**	**16**	**18**
Center Sample	**13**	**23**	**32**	**36**
Multiple Sample	**40**	**52**	**NA**	**63**

Percent Acceptance Rate

Algorithm Performance Comparison
40K FRUIT/Second (-5dB to +10dB)
(Taken from SICASP/WG-1 WP/1/554 9 October 1996
Improved Squitter Reception Techniques
Prepared by Dr. Jeffrey L. Gertz and Dr. Vincent A. Orlando)