

RTCA Special Committee 186, Working Group 3

ADS-B 1090 MOPS

Meeting 2

ACTION ITEM 1-6

Review of Appendix I

Presented by Vincent Orlando

SUMMARY

At the first Rev A meeting of WG-3, it was noted that Appendix I covered a number of topics but did not define the configuration used as the basis for the MOPS requirements for enhanced squitter reception.

This working paper proposes changes to Appendix I to address this concern.

1.0 Background

Appendix I to DO-260 contains a description of a number of techniques that can be used to improve the reception of squitters that are overlapped with ATRBS fruit. A main focus of Rev A to DO-260 is to add requirements and test procedures for improved squitter reception. The approach will be to add requirements and test procedures for the improved processing, without specifying the technique to be used.

2.0 Problem

At the December meeting of WG-3 it was noted that Appendix I did not specify the configuration of improved processing that would be used as the basis for specifying MOPS performance requirements.

3.0 Proposed Revision to Appendix I

The following pages propose modifications to Appendix I to clarify the configuration used to develop the MOPS requirements for the performance of the improved reception techniques.

I.1

Purpose and Scope

The purpose of this appendix is to provide a description of improved squitter reception techniques. Elements of improved squitter reception include (1) the use of amplitude to improve bit and confidence declaration accuracy, (2) more capable error detection/correction algorithms, (3) more selective preamble detection approaches, and (4) combinations of the above.

The improved techniques presented in this appendix represent one way of achieving the performance requirements specified in para TBD for enhanced squitter reception. The exact squitter processing configuration used as the basis for these performance requirements is specified in section I.5

The ~~current~~ reception techniques, as required in section 2.2.4.3.4 of this MOPS, are also described in this appendix for comparison with the enhancements.

I.4.3.4

Brute Force Error ~~Detection and~~ Correction Technique

If the bit declaration algorithm has performed its function properly, all errors in Mode S data values will reside in bits declared low confidence. If this is true, a simple approach to error correction is to try all possible combination of low confidence bits, and accept the set that matches the error syndrome (provided only one success is discovered). For obvious reasons, this method has been named the Brute Force Technique. It is applicable to any method of data and confidence declaration, with or without amplitude, and is applied after the other techniques have failed.

~~The process proceeds as follows. Error detection is applied first. If the message passes, the process ends, and the message is delivered. If an error is detected, then conservative error correction is applied, and if a correction results, then the process ends, and the message is delivered. If the constraint for conservative correction is not satisfied (section I.4.3.2), then the brute force technique is applied. More generally, the brute force technique can be applied as a follow-on to any of the other techniques.~~

Implementation of ~~this~~the brute force -technique depends upon the fact that each Mode S bit position corresponds to a unique syndrome, and that sets of bits produce a syndrome that is the exclusive OR of all individual bit syndromes. For example, if bit 1 is the only bit declared in error, the error syndrome at the receiver will be hex 3935EA, while bit 31 produces hex FDB444, and bit 111 has syndrome hex 000002. Thus if those three bits are all declared in error, the error syndrome will be calculated to be hex C481AC. The table of individual bit syndromes is pre-calculated and stored in the receiver.

It is possible for two or more subsets of the low confidence bits to match the syndrome. In such cases, the message is rejected, and no harm is done. However, if a high confidence bit has been declared in error, and a single subset of the low confidence bits matches the syndrome, the message will be "corrected" to the wrong message, producing an undetected error. (If no subset matches the syndrome, it must be true that a high confidence bit error has been made, and the message is rejected.)

Clearly, for processing time and error bounding reasons, the maximum number of low confidence bits to process must be limited. The number of cases to consider is given by 2^n if n low confidence bits exist for a message; this grows exponentially with n (32 at $n = 5$, 4096 at $n = 12$). The undetected error rate is proportional to the number of cases, and thus also grows exponentially with n . Fortunately, the Hamming distance of 6 for the Mode S parity code implies that undetected errors are essentially zero if $n \leq 5$ is enforced. For this reason, a value of $n = 5$ has been used in the development of the brute force algorithm.

I.5

For improved reception performance in a high fruit environment, the optimum configuration has been found to be:

1. Enhanced preamble detection (I.4.1)
2. Bit and confidence declaration based on the 4-4 multiple amplitude approach. (I.4.2.4)
3. Error detection using the Mode S 24-bit CRC technique. (Ref).
4. First pass error correction using the conservative technique (I.4.3.2)
5. Second pass error correction using the brute force technique with n=5 (I.4.3.4)

The process proceeds as follows. Preamble detection and bit and confidence declaration are performed. Next, Mode S error detection is applied. If the message passes, the process ends, and the message is delivered. If an error is detected, then conservative error correction is applied, and if a correction results, then the process ends, and the message is delivered. If the constraint for conservative correction is not satisfied, then the brute force technique is applied.

The above configuration was used as the basis for the performance required for enhanced squitter reception as specified in section TBD.

I.6 Summary

New techniques have been developed for enhancing reception of Extended Squitters in environments of high interference. The new techniques include improvements in preamble detection, improvements in declaration of information bits and confidence bits within the squitter message, and improvements in error detection/correction.

These developments were originally carried out using pulse-level simulation to assess the resulting performance. Subsequently flight tests have been conducted using these techniques, making comparisons relative to the current techniques. Both the simulation and flight test results indicate that substantial improvements in performance are achievable using these techniques when operating in an environment of high interference.

~~A planned version 2 of this MOPS will include quantification of the performance using these techniques, and will include avionics requirements and supporting tests for including these techniques in certain classes of avionics.~~