

RTCA Special Committee 186, Working Group 3

ADS-B 1090ES MOPS

Meeting #19

**RTCA, Washington DC
7 December 2005**

Identified Errors in Test Procedures in DO-260A 2.4.4.4

(Prepared by John Van Dongen, FAA Technical Center, ACB-130)

SUMMARY

Four Test Procedure Steps contained in DO-260A sections 2.4.4.4.2.2 and 2.4.4.4.2.3 are incorrect such that properly designed equipment will fail these tests as currently defined. This Working Paper documents these errors, but solutions have not been yet been developed.

Introduction

After conducting test procedures as defined in ADS-B MOPS DO-260A section 2.4.4.4 Verification of Enhanced Squitter Reception Techniques, it has been determined that some of the test procedures contain errors. The errors were found in section 2.4.4.4.2.2 Four-Pulse Preamble Detection Tests and section 2.4.4.4.2.3 Preamble Validation Tests. The test procedures defined in these sections were conducted both at the FAA Technical center and JHU APL to test Enhanced Squitter Reception Techniques that were developed according to the MOPS Appendix I. Some of these test procedures resulted in common failures with both decoder implementations. Analysis revealed that the decoders were acting properly and that the test procedures were in error. This paper presents the data from conducting the tests and an analysis of why the tests are in error. Resolutions to the test procedure errors are not offered at this time pending further testing.

Section 2.4.4.4.2.2 Four-Pulse Preamble Detection Tests

DO-260A section 2.4.4.4.2.2 contains Four-Pulse Preamble Detection Tests that are intended to verify that the ADS-B reply processor correctly detects the presence of a valid ADS-B preamble whose pulse characteristics are within allowable limits and rejects preambles having pulse position and width characteristics that are outside the allowable limits. There are 7 different preamble pulse input variations (Input A through Input G) that are tested at two different power levels (-23 and -65 dBm). The results of these tests are shown in Table 1.

TABLE 1 – DO-260A 2.4.4.4.2.2 PREAMBLE TEST RESULTS

Input Power (dBm)	PREAMBLE TEST	Input	Req. Reply Rate	Tech Center Measured Reply Rate	APL Measured Reply Rate
-23	2.4.4.4.2.2-01	A	>= 90	100	100
-23	2.4.4.4.2.2-03	B	>= 90	100	100
-23	2.4.4.4.2.2-05	C	<=10	0.05	0
-23	2.4.4.4.2.2-07	D	<=10	64.75	48
-23	2.4.4.4.2.2-09	E	<=10	100	100
-23	2.4.4.4.2.2-11	F	<=10	100	100
-23	2.4.4.4.2.2-13	G	<=10	0	0
-65	2.4.4.4.2.2-02	A	>= 90	100	100
-65	2.4.4.4.2.2-04	B	>= 90	100	100
-65	2.4.4.4.2.2-06	C	<=10	0.15	0
-65	2.4.4.4.2.2-08	D	<=10	76.85	41
-65	2.4.4.4.2.2-10	E	<=10	100	100
-65	2.4.4.4.2.2-12	F	<=10	100	100
-65	2.4.4.4.2.2-14	G	<=10	0	0

Both Enhanced Receiver implementations failed the tests with inputs D, E, and F as highlighted in *red*. In these three cases, the decoder is required to reject the preamble and reply at a rate of 10% or less. It was determined that the test procedure input criteria D, E, and F are in error because the preamble pulse characteristics defined do not position the preamble pulses outside the allowable limits as intended. Following is an explanation of the problem with the three test input configurations.

Input D

Test input D positions the last three preamble pulses (P2, P3 & P4) 0.2 microseconds later than the nominal position. The test requires that the equipment accepts 10% or less of the input signal. Although there is no specific explanation of the intent of this test procedure, it appears to test the requirement that the preamble detector provide a plus-or-minus 1-clock (0.1 microseconds with a 10 MHz sample rate) maximum sample tolerance for pulse detection. Figure 1 illustrates the preamble pulse configuration according to input D.

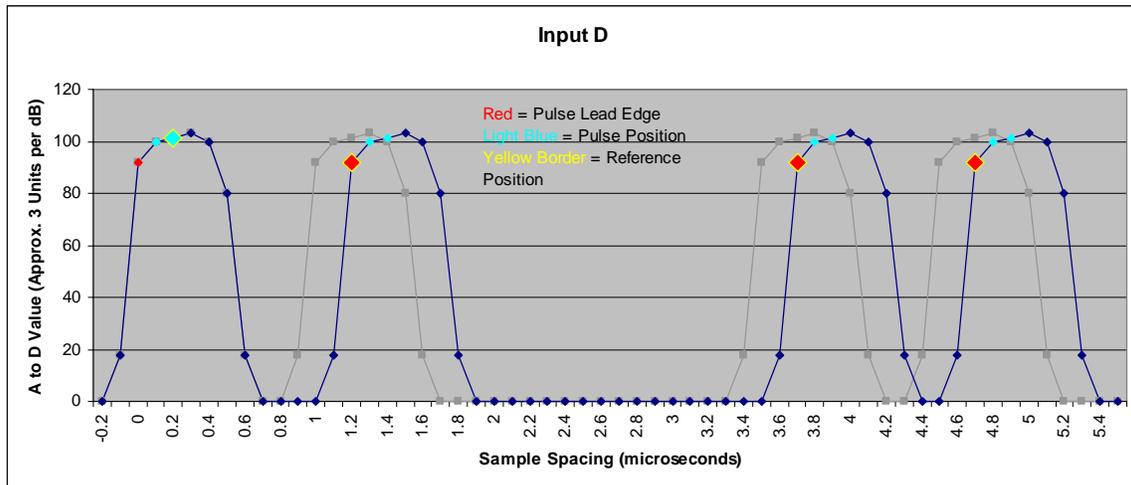


Figure 1 – Four-Pulse Preamble Detection Test 2.4.4.4.2.2-7 & 8, Input D Pulse Sample Example

In Figure 1 and subsequent figures, the log video samples that meet the criteria for the pulse leading edge appear in red, the samples that meet the criteria for a pulse position appear in light blue, and all remaining samples are dark blue. Those samples that align with the reference position are enlarged with a yellow border. The gray background samples indicate a nominal preamble pulse configuration. (Note: The receiver threshold is set to A-To-D value of 20 in these examples)

The example illustrated in Figure 1 shows why the preamble pulse configuration is still accepted even with three of the pulses at +0.2 microseconds out of position. The reference position shifts to the 3 leading edges of the delayed pulses (highlighted in red), and although the first pulse leading edge is not in detectable range of the reference

position, there are subsequent “pulse position” samples in the first preamble pulse that satisfy the preamble detector. Since there are more than the required 2 pulse leading edges detected, and a “pulse” was located in all four preamble pulse positions, the preamble detection is successful.

It is important to consider that the sample configurations illustrated in these figures are examples only and that there is some variation in the number of and location of samples that are categorized as pulse positions or leading edges. Often there are more than three samples per pulse that are either a leading edge or pulse position (often the sample preceding the leading edge is also a pulse position) and other factors such as pulse rise and decay times, threshold level, and receiver bandwidth will affect the log video signal. Also how the incoming signal aligns with the digital sampler will cause variations as well (a different sample rate would obviously have even more of an effect). For these reasons it may not be possible to select a Δ position that is always exactly 1 sample out of range of detection.

Using the test as it is currently defined, the test results with input D, although much higher than the maximum required 10%, were not 100%. It has not been determined exactly why the preamble is not always detected with this input although it could be due to the sample variations described above and/or that since the resulting shift in the reference position misaligns the data block decoder by 0.2 microseconds, the data block decoding may not always be successful.

Inputs E and F

Inputs E and F can be discussed together because they are the same test as each other that just involve different pulses of the preamble. The problem cause and effect are the same. Inputs E and F each alter a normal preamble pulse configuration by shifting one of the preamble pulses early by 0.125 microseconds and another late by 0.125 microseconds. The test requires that the equipment accepts 10% or less of the input signal. Again, there is no specific explanation of the intent of these test procedures, but it appears that the intent is to test the requirement that the preamble detector allow a + or – 1 sample position tolerance, *but not both* in a given preamble. Figures 2 and 3 illustrate the preamble configurations for test inputs E and F respectively.

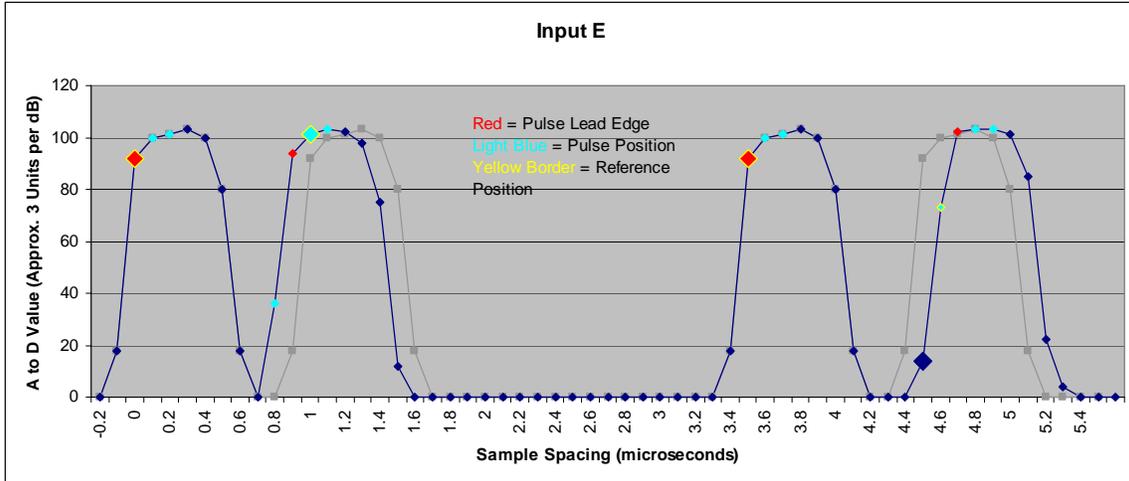


Figure 2 – Four-Pulse Preamble Detection Test 2.4.4.4.2.2-9 & 10, Input E Pulse Sample Example

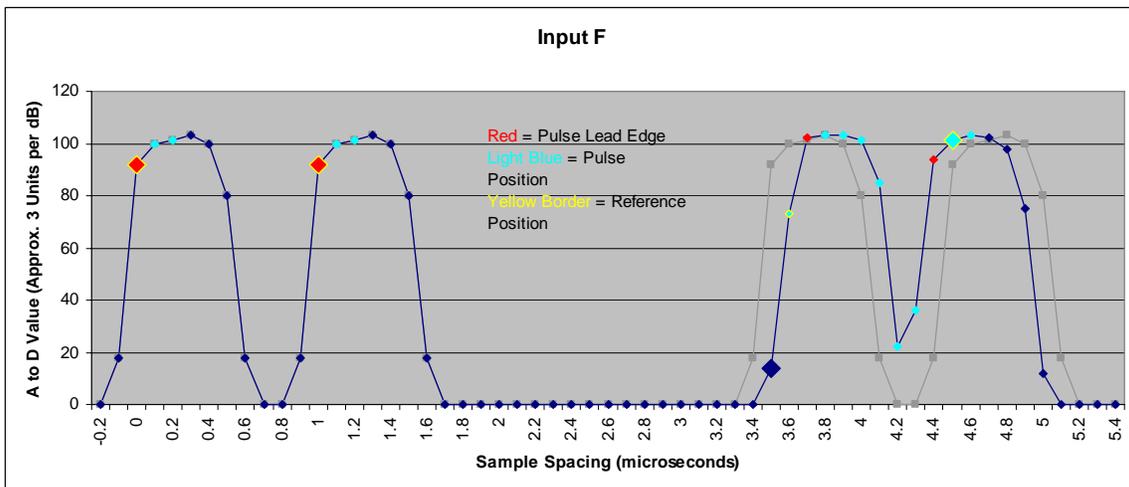


Figure 3 – Four-Pulse Preamble Detection Test 2.4.4.4.2.2-11 & 12, Input F Pulse Sample Example

When inputs E and F were injected into the enhanced receivers at the Tech Center and APL, the reception rate was 100%. The altered preambles are not rejected because they still meet the criteria for detection. In each case the reference position is set by the leading edge of the 2 unaltered pulses. The pulses that were altered still have pulse position samples aligned within 1 sample of the preamble detector, and it is not required to shift in both directions to detect them. A corrected test procedure would position pulses such that at least one pulse must have a negative clock shift to be accepted (the trail edge of the pulse should be located nearer to the nominal position of where the leading edge is supposed to be), while another pulse must have a positive clock shift to be accepted. It might not be possible to define pulse positions that guarantee that one pulse is always +1 sample and another -1 sample from the reference position.

Section 2.4.4.4.2.3 Preamble Validation tests

Test procedure 2.4.4.4.2.3 attempts to verify that the receiver rejects signals with one of the five data bits used for preamble validation (the first 5 bits of the data block) set below the threshold for detection, and accepts signals if the 6th bit is below the threshold. The threshold is set to 6 dB below the amplitude level of the preamble by the receiver. The test procedure calls for setting the amplitude of each of the first 6 data bits independently to -7 dB relative to the rest of the transmission and verifying that the signal is rejected when one of the first 5 bits are at the reduced level, and accepted when the 6th bit is at the reduced level. Each bit is tested at 2 power levels (-23 dBm with reduced pulse at -30 dBm, and -65 dBm with reduced pulse at -72 dBm) for a total of 12 test steps. The test calls for using a DF code of 17.

The problem with this test procedure is with steps 7 through 10 where it is required to independently lower the amplitude of the 4th or 5th bit. With a DF code of 17, the 4th and 5th bits are one pulse. The equipment at used at the Tech Center (and presumably most amplitude modulating test equipment) is unable to transmit a single pulse with each half at different amplitudes (at least at a speed fast enough so that the amplitude transition is complete between 2 samples that are 0.1 microseconds apart). APL conducted this test with simulation and was able to control the amplitude of the 4th and 5th bit independently. However, the receiver did not reject the signal even then because at least 1 sample of the reduced bit adjacent to the higher amplitude half was still above the threshold (it only takes 1 sample of the chip to pass validation). This occurred because the simulated bandwidth effects slowed the amplitude transition and the reduced signal amplitude was only 1 dB below the threshold.