

RTCA Special Committee 186, Working Group 3

ADS-B 1090 MOPS, Revision A

Meeting #13

**Action Item 12-5
Revised Appendix I Section 4.2 Enhanced Bit and Confidence
Declaration**

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SUMMARY

This revision to Appendix I places the “multiple sample without table lookup” method for bit and confidence declaration as the first in the discussion of multi-sample techniques. This is in accordance with Action Item 12-5. In addition, the text is also revised to use a 10 MHz default sampling rate with all techniques. This was done to be consistent with the proposed changes to the enhanced preamble detection material in 1090-WP-13-13.

I.4.2 Enhanced Bit and Confidence Declaration

I.4.2.1 Overview

The current technique of declaring a bit based upon the higher of the two chips will generate bit errors in cases of higher level overlapping Mode A/C fruit (Figure I-2, part c). The use of amplitude to correlate the received pulse with the preamble pulse level will improve bit declaration accuracy. Four techniques have been investigated. One is a very simple approach that uses only the amplitude measured at the center of each chip. The remaining three use a more capable approach that takes advantage of ~~all the four~~ samples per chip that are taken ~~in the current technique~~ to establish bit and confidence. Each of these techniques is described in the following paragraphs.

The following description of the center sample technique is intended to provide an example of processing performance needed to meet the requirements of Class A1 equipment. This description also serves as an introduction to the three more capable approaches. The center sample technique will not provide sufficient performance to meet requirements specified for Class A2 and A3 equipment in the test procedures of §2.4.4.4. The specified performance for these latter classes of equipment can only be met by an approach that performs equivalently to one of the multi-sample techniques.

I.4.2.2 Use of Center Amplitude

An improvement in the declaration of Mode S data bits can be achieved if the actual amplitudes of the center samples of the '1' and '0' chips can be measured for each data position, rather than just a comparison of which chip sample is greater. All Mode S pulses, including those of the preamble, have approximately the same level (within 1 or 2 dB). Thus if the preamble level is measured, the expected level of each data pulse will be known. Then if both center samples of a data position are above threshold, but only one is within a ± 3 dB band centered at the preamble level, it would be reasonable to assume that the corresponding chip is the correct Mode S pulse location. This is illustrated in Figure I-2, part d.

Figure I-3 illustrates the new data and confidence declaration algorithms that result when the actual sample amplitudes can be measured, and both samples are above threshold. As shown in Figure I-3, a bit is high confidence when 1 and only 1 of the two samples correlate with the preamble level. The correlating sample, rather than the larger sample, is declared to be the true data value. If both samples, or neither sample, correlates with the preamble, a low confidence bit is declared. In this case, the larger sample is selected as the bit value, as in the current technique.

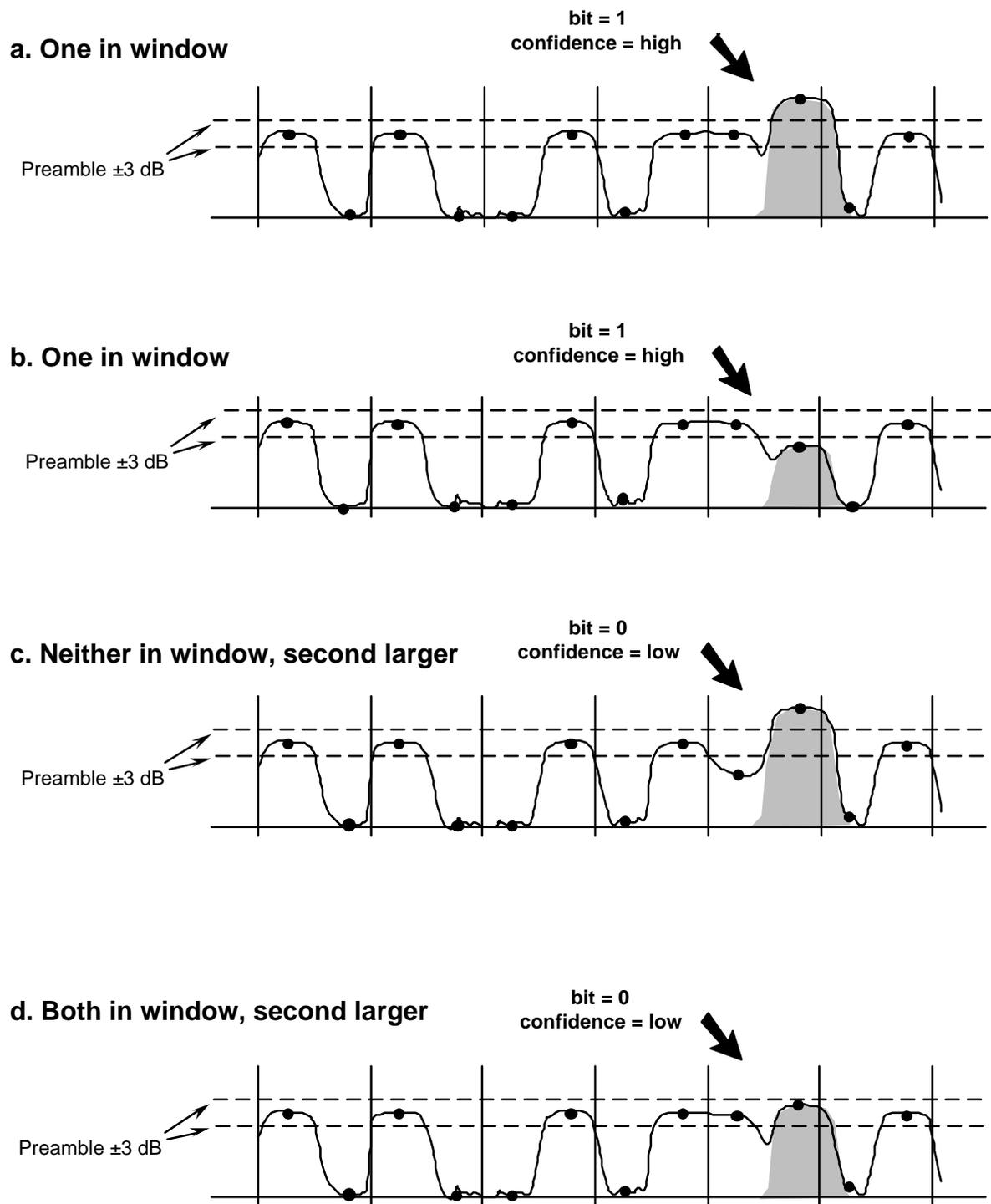


Figure I-3: Center Amplitude Bit and Confidence Declaration

The major advantage of this scheme is the significant reduction in low confidence and bit errors generated for the Mode S message. Presently, any data position with both samples above threshold is declared low confidence. This translates to a low confidence declaration whenever an above-threshold Mode

A/C fruit overlaps a Mode S empty chip position. If the Mode A/C signal is of greater power, the bit position is declared in error.

With the center amplitude technique, a low confidence bit is declared only when the Mode A/C fruit is within 3 dB of the Mode S signal. Mode A/C fruit of either lower or higher power in general cause neither errors nor low confidence bits. Thus the region of concern for Mode A/C aircraft is reduced from all the aircraft at closer range to just those at approximately co-range. This is particularly significant when the system is attempting to listen to far-range Mode S aircraft.

It is occasionally possible for this new algorithm to produce high confidence bit errors. The most likely case occurs when two Mode A/C pulses overlay the same Mode S bit position. If one overlaps the data pulse, and drives its sample out of the preamble window, then an error will result if the other Mode A/C pulse lands on the other chip and its amplitude is within the preamble window. Such occurrences will in general create a rejected message, rather than an undetected error.

I.4.2.3 Use of Multiple Amplitude Samples

The above amplitude data declaration approach can be improved if all ~~108~~ samples (~~54~~ per chip) that are taken for each Mode S bit position are utilized in the decision process. In particular, the event of both center samples within the preamble window can often be resolved. For example, consider the typical such situation depicted in Figure I-2, part e. *(Temporary note: Figure I-2 will need to be updated to reflect a 10 MHz sample rate).* Although both center samples are within the window, the fact that the earlier chip has all samples within the window, whereas the later chip has several samples below the window suggests that the signal is present in the earlier chip. This error situation can often be rectified when all ~~108~~ samples are examined. Also, in some cases when an interference pulse overlaps a signal pulse, the small frequency difference will produce variations in amplitude, whereas the signal by itself would be more constant, and such patterns can be useful in declaring the bit and confidence.

~~To take advantage of these differences between a pure signal and a combination of signal plus interference, a technique was developed based on a lookup table, whose contents are derived from many runs of a simulation. Specifically, each of the 8 samples is quantized into four levels:~~

~~0: below threshold (-6 dB relative to the preamble)~~

~~1: above threshold but below the +/- 3 dB preamble window~~

~~2: within the +/- 3 dB preamble window~~

~~3: above the +/- 3 dB preamble window~~

I.4.2.3.1

Baseline Multi-Sample Technique ~~Without Table Lookup~~

Temporary Note (working paper only): This entire section has, for the most part been re-written although it is not highlighted as having been changed.

The multi-sample enhanced bit and confidence declaration technique makes use of all 10 samples for each Mode S bit position to determine the bit and confidence values. Sample amplitudes in each chip are compared to the amplitude reference level established by the preamble to quantify the number of samples in each chip that a) match the preamble amplitude indicating the presence of a pulse, or b) are significantly lower in amplitude indicating a lack of transmitted energy.

The first step is to establish an amplitude window that will include samples that are within +/- 3 dB of the preamble reference level and a minimum amplitude threshold set to 6 dB below the reference level. Samples that fall within the window are considered to match the preamble and samples that are below the minimum threshold are considered to indicate a lack of transmitted energy. The samples are categorized as follows:

A: within the +/- 3 dB preamble window

B: below threshold (6 dB or more below the preamble)

The second step is to count the number of samples in each chip that are of each category. Less weight is given to the samples near the transitional areas of each chip (the transitional samples are the first and last samples of each chip). To facilitate this, samples other than those at each end count double. Therefore, with weighting factored in and a 10 MHz sampling rate, the counts for each category will range from 0 to 8 for each chip (1 sample at each end + 3 samples in-between x 2). The four counts are summarized as follows:

1ChipTypeA = #of weighted samples in the 1 chip of type A (Match Preamble)

1ChipTypeB = #of weighted samples in the 1 chip of type B (Lack energy)

0ChipTypeA = #of weighted samples in the 0 chip of type A (Match Preamble)

0ChipTypeB = #of weighted samples in the 0 chip of type B (Lack Energy)

Next, two equations using the above counts will produce two scores that indicate how well the sample pattern matches a transmitted 0 and how well the sample pattern matches a transmitted 1. The equations are as follows:

$$1\text{Score} = 1\text{ChipTypeA} - 0\text{ChipTypeA} + 0\text{ChipTypeB} - 1\text{ChipTypeB}$$

$$0\text{Score} = 0\text{ChipTypeA} - 1\text{ChipTypeA} + 1\text{ChipTypeB} - 0\text{ChipTypeB}$$

The highest score determines the bit value. In the case of a tie, the bit defaults to zero. If the difference is 3 or more the bit is high confidence. The confidence threshold of 3 was determined by testing the algorithm with a 10 MHz sampling rate with thousands of iterations with a high fruit rate. If the algorithm is applied with a different sampling rate, the appropriate confidence threshold may need to be determined under similar test conditions.

I.4.2.3.2 Alternate Multi-Sample Technique With Full Table Lookup

To take advantage of the differences between a pure signal and a combination of signal plus interference, a technique was developed based on a lookup table, whose contents are derived from many runs of a simulation. Specifically, each of the 10 samples is quantized into four levels:

0: below threshold (-6 dB relative to the preamble)

1: above threshold but below the +/- 3 dB preamble window

2: within the +/- 3 dB preamble window

3: above the +/- 3 dB preamble window

Since there are 108 samples, with 4 possible values each, a Mode S data position can have $4^8 - 4^{10} = 104857665536$ (~~64K1M~~) different sample patterns. Two 1-bit tables, each stored in a 64K1M x 1 ROM, are defined over the set of patterns: the first declaring the bit position to be a '1' or '0', the second high or low confidence. Once the pattern existing for a given bit is determined, two table lookups supply the proper declaration. If higher sampling rates are used, the number of sample patterns and the table size will increase exponentially.

These tables are generated by running millions of simulations of Mode S messages in 40,000 fruit per second environments. For each bit of each trial, the pattern and the correct Mode S bit value are noted. The result could be, for example, 5876 examples of pattern 16453, of which 5477 occurred when the Mode S bit was a "1." The table values are then defined as follows, assuming an "uncertainty parameter" value of 10%:

- H1: 90% or more of the samples occurred when the bit was a '1'
- L1: 50% - 90% of the samples occurred when the bit was a '1'
- L0: 10% - 50% of the samples occurred when the bit was a '1'
- H0: 10% or fewer of the samples occurred when the bit was a '1'.

Since pulse shapes are critical to this method, live data verification of the table entries is required to establish these values.

I.4.2.3.3 **Alternate Multi-Sample Technique With Reduced Table Lookup**

The above 108 sample approach requires lookup tables of size 1M64K, adding cost to the hardware implementation of the decoder. A variation of this method that only requires tables of size 2561K, called the 4-45-5 approach, has been designed to reduce this expense.

The 4-45-5 method forms two estimates of the bit data and confidence values, one using the odd samples (1-3-5-7-9) and the other using the even samples (2-4-6-8-10); the final decision is then a combination of the individual estimates. Since each set includes samples in both chip positions, pattern matching is still possible, although the fineness of the pattern variation is cut in half. Since only 45 samples are in each set, and each sample is quantized to the same 4 levels as above, $4^4 \cdot 4^5 = 2561024$ patterns are possible for each set.

To counteract the loss of resolution, and to aid in the combining operation, 3 levels of confidence (high, medium, and low) are defined for each pattern. Following the simulation generation scheme described above, the table values are defined as follows:

- H1: 90% or more of the samples occurred when the bit was a '1'
- M1: 70% - 90% of the samples occurred when the bit was a '1'
- L1: 50% - 70% of the samples occurred when the bit was a '1'
- L0: 30% - 50% of the samples occurred when the bit was a '1'
- M0: 10% - 30% of the samples occurred when the bit was a '1'
- H0: 10% or fewer of the samples occurred when the bit was a '1'.

The values of 10% and 30% are parameters; the value of 30% was selected to provide the performance discussed below. Since 3 confidence levels now exist, the confidence lookup table for each sample set is sized ~~1024~~~~256~~¹⁰²⁴~~x2~~. The total table requirement for data and confidence, for the two sample sets, is thus ~~256~~~~1024~~¹⁰²⁴~~x6~~.

Once the values and confidences are determined for each set of samples, odd and even, the composite values actually declared for the bit are found according to Table I-1.

Table I-1: Combining Odd and Even Outputs

Odd	Even					
	H1	M1	L1	H0	M0	L0
H1	H1	H1	H1	L0	H1	H1
M1	H1	H1	L1	H0	L0	L1
L1	H1	L1	L1	H0	L0	L0
H0	L0	H0	H0	H0	H0	H0
M0	H1	L0	L0	H0	H0	L0
L0	H1	L1	L0	H0	L0	L0

Note that if either sample set is high confidence, that set's data value rules unless the samples conflict and are both high confidence. Also notice that two agreeing medium confidence samples produce a high confidence result. With the parameter for medium confidence set at 30%, the probability of error for medium confidence agreement is $0.3 \times 0.3 = 0.1$, which matches the ~~8~~¹⁰ sample probability of error for a high confidence decision. Finally, when the sample decisions conflict at the same confidence level, a low confidence 0 is declared for lack of a better estimate.

If a sampling rate ~~higher~~^{other} than ~~8~~¹⁰ MHz is used, the number of samples from the odd and even samples ~~and the resulting table sized~~ will ~~be adjusted~~^{increase} accordingly, ~~and the table size will increase exponentially~~. For example, if a ~~8~~¹⁰ MHz sampling rate is used, there are ~~5~~⁴ samples in each set, and each sample is quantized to the same 4 levels as above, ~~4⁵ - 4⁴ = 256~~¹⁰²⁴ patterns are possible for each set. The total table requirement for data and confidence, for the two sample sets, is thus ~~256~~¹⁰²⁴~~x6~~. If a 16 MHz sampling rate is used, there are 8 samples in each set, and each sample is quantized to the same 4 levels as above, $4^8 = 65,536$ (64K) patterns are possible for each set. The total table requirement for data and confidence, for the two sample sets, is thus 64Kx6. Once the values and confidences are determined for each set of samples, odd and even, the composite values are declared according to Table I-1 independent of the sampling rate.